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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/932,055	08/16/2001	Simon Dodd	10007744-1	5019

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EXAMINER	
UMEZ ERONINI, LYNETTE T	

ART UNIT	PAPER NUMBER
1765	

DATE MAILED: 08/06/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/932,055	DODD, SIMON	
	Examiner	Art Unit	
	Lynette T. Umez-Eronini	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) *11-22* is/are withdrawn from consideration.

5)☒ Claim(s) *1-10 and 23-26* is/are allowed.

6)☒ Claim(s) *11-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *11-22* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Request for Continued Examination

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on June 8, 2004 has been entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 11 and 14 are rejected under 35 U.S.C. 102(e) as being anticipated by Kawamura et al. (US 6,543,884 B1).

Kawamura teaches, " . . . Thin film layers, including ink ejection elements (same as applicant's drop generator), are formed on a top surface of a silicon substrate. The various layers are etched to provide conductive leads to the ink

ejection elements. At least one ink feed hole is formed through the thin film layers for each ink ejection chamber. A trench is etched in the bottom surface of the substrate so that ink can flow into the trench and into each ink ejection chamber through the ink feed holes formed in the thin film layers. An orifice layer is formed on the top surface of the thin film layers to define the nozzles and ink ejection chambers. A phosphosilicate glass (PSG) layer, providing an insulation layer beneath the resistive layers, is etched back from the ink feed holes and is protected by a passivation layer to prevent the ink from interacting with the PSG layer (Abstract). FIGS. **4**, **8**, and **10**A – **10**E, and **11** show a plurality of thin films (column 4, lines 19-21), which comprises: FOX **92**, PSG **92**, TaAl **62**, Si_3N_4 **96,** SiC **98**, Ta **100**, and Au **114**. The aforementioned reads on,

A method of fabricating multiple layer of a thermal injet printhead that includes a substrate and a trench for moving ink across the substrate, as well as drop generator components for ejecting drops of ink form the substrate, comprising the steps of:

providing a layer on the substrate to serve as a drop generator component; and then etching the substrate to form the trench in the substrate.

Since Kawamura teaches the using the same materials in forming layers on a substrate as the claimed invention, then using Kawamura method of forming a layer on a substrate in the same manner as the claimed invention would result in a layer on the substrate to serve as a mask to define the trench for etching.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kawamura (US '884 B1) as applied to claim 11 above.

Kawamura differs in failing to teach growing a layer of oxide to serve as a transistor gate component of the drop generator as well as the mask.

It would have been obvious to one having ordinary skill in the art at the time of the claimed invention to use a conventional method of forming a gate electrode by growing or depositing an oxide layer on a semiconductor in fabricating a transistor, which comprises a source region, drain region, and gate electrode and using a conventional photolithographic method in growing a silicon oxide layer to form a hard mask.

6. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kawamura (US '884 B1) as applied to claim 1 above, and further in view of Hawkins (US 4,863,560).

Kawamura differs in failing to teach capping the oxide layer near the trench with a layer of passivation material.

Hawkins teaches a SiO_2 **26** layer is lithographically processed to form a via **23** on a silicon wafer **19**; a Si_3N_4 layer **28** is deposited over the patterned SiO_2 **26** layer and the exposed silicon wafer surface **22** and the Si_3N_4 layer **28** is then lithographically processed to produce via **24**, so that via **24** exposes the bare silicon surface **22** of wafer **19**. Hawkins further teaches, "Note that a border **29** of Si_3N_4 (see FIG. 5) is left about 1 mil wide inside of the SiO_2 via **23** both for protection and limitation of undercutting during subsequent ODE (orientation etching) processing (column 5, lines 43-64), which reads on, capping the oxide layer near the trench with a layer of passivation material.

It would have been obvious to one having ordinary skill in the art at the time of the claimed invention to modify Kawamura by using Hawkins method of capping an oxide layer near the trench for the purpose of protection and limitation of undercutting during subsequent ODE processing (column 5, lines 61-64).

Response to Arguments

7. Applicant's arguments filed June 8, 2004 have been fully considered but they are not persuasive. Applicant traverses the 103 rejection of claims 11-14 and argues Kawamura fails to teach or suggest providing on the substrate a layer to serve both as drop generator component and as a mask to define the trenches for etching, in claims 11 and 14; fails to support an oxide layer be used to form a transistor, but the same oxide layer must act as a mask, in claim 12; and fails to overcome the rejection of claim 13 by combining Haskins.

Applicant's arguments is unpersuasive because Kawamura teaches ink ejection elements (same as applicant's drop generator), are formed on a top surface of a silicon substrate, a trench is etched in the bottom surface of the substrate so that ink can flow into the trench and into each ink ejection chamber through the ink feed holes formed in the thin film layers, a phosphosilicate glass (PSG) layer, providing an insulation layer beneath the resistive layers, is etched back from the ink feed holes and is protected by a passivation layer to prevent the ink from interacting with the PSG layer (Abstract). Since Kawamura teaches the using the same materials in forming layers on a substrate and uses the same method of etching a trench in the substrate as claimed by applicants, then using Kawamura method of forming a layer on a substrate in the same manner as the claimed invention would result in a layer on the substrate to serve as a mask to define the trench for etching as well as growing an oxide to serve as a transistor gate component of the drop generator as well as the mask.

Since Hawkins teaches a SiO_2 **26** layer is lithographically processed to form a via **23** on a silicon wafer **19**; a Si_3N_4 layer **28** is deposited over the patterned SiO_2 **26** layer and the exposed silicon wafer surface **22** and the Si_3N_4 layer **28** is then lithographically processed to produce via **24**, so that via **24** exposes the bare silicon surface **22** of wafer **19** and further teaches, "Note that a border **29** of Si_3N_4 (see FIG. 5) is left about 1 mil wide inside of the SiO_2 via **23** both for protection and limitation of undercutting during subsequent ODE (orientation etching) processing (column 5, lines 43-64), then the said above reads on, capping the oxide layer near the trench with a layer of passivation

material. Hence, it would have been obvious to one having ordinary skill in the art at the time of the claimed invention to modify Kawamura by using Hawkins method of capping an oxide layer near the trench for the purpose of protection and limitation of undercutting during subsequent ODE processing (column 5, lines 61-64).

Allowable Subject Matter

8. Claims 1-10 and 23-26 are allowed.

9. The following is a statement of reasons for the indication of allowable subject matter:

As to claims 1, 2, and 4, applicants have presented persuasive arguments (see Remarks of June 8, 2004, page 8) to show the prior art of record taken alone or in combination fails to teach, suggest, or render obvious masking a first portion of a substrate surface with passivation material having edges that define boundaries on the substrate surface such that within the boundaries a second surface portion is exposed for etching, in combination with the other limitations of the said claims;

As to claim 3, the prior art of record taken alone or in combination fails to teach, suggest, or render obvious masking a substrate surface with the passivation material includes simultaneous deposition of the passivation material at a location away from the exposed surface portion to enable use of some of the passivation material as one of the drop generator layers as well as the mask, in

the sequence of steps in a method of etching a substrate surface, along with the other limitations of the said claim;

As to claim 5, the prior art of record taken alone or in combination fails to teach, suggest, or render obvious the sequence of steps: comprising masking a first portion of a substrate surface with passivation material having edges that define boundaries on the substrate such that within the boundaries a second surface portion is exposed for etching; depositing a metal layer over the passivation material; and then etching the second surface portion, in combination with the other limitations of the said claim;

As to claims 6-10, applicants have presented persuasive arguments in Remarks (filed 6/8/2004, on pages 9-10), which show the prior art of record taken alone or in combination fails to teach, suggest, or render obvious a method of masking and etching a surface of a silicon substrate, comprising the steps of: providing on the substrate surface a patterned oxide layer having edges that define boundaries of a surface portion such that within and adjacent to the boundaries the surface portion is exposed for etching; covering the oxide layer near the edges with passivation material; and etching the entire surface portion of the silicon substrate that is exposed for etching, in combination with the other limitations of the above claims; and

As to claims 23-26, the prior art of record taken alone or in combination fails to teach, suggest, or render obvious a method of etching a substrate surface comprising: depositing a passivation material on a first portion of the substrate surface and subsequently removing a portion of the deposited passivation

material from a second portion of the substrate surface within the first portion, such that the second portion is free of passivation material; depositing a metal over the passivation material; and etching the second portion, in claim 23 and in combination with the rest of the limitations of claims 24-26.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lynette T. Umez-Eronini whose telephone number is 571-272-1470. The examiner is normally unavailable on the First Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on 571-272-1465. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ltue

July 29, 2004

NADINE G. NORTON
SUPERVISORY PATENT EXAMINER